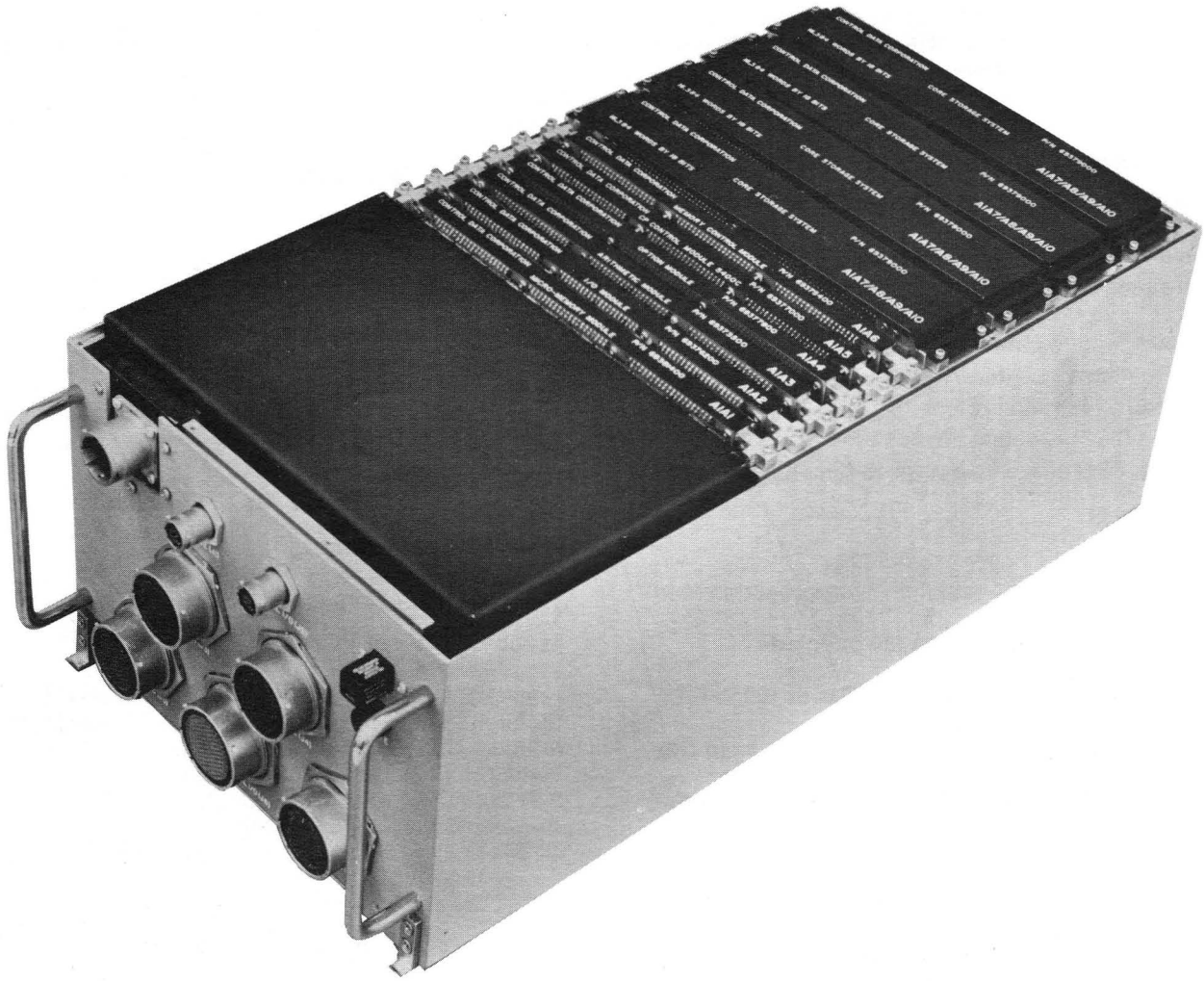
CONTROL DATA®
ADVANCED MICROPROGRAMMABLE PROCESSOR

CONTROL DATA
CORPORATION



The CONTROL DATA Advanced Microprogrammable Processor (AMPP) provides a versatile solution to advanced processor requirements of the mid-1970's and beyond. The AMPP combines microprogrammed control with state-of-the-art circuit construction and a 750-nanosecond core memory in a MIL-E-5400 Processor, capable of executing more than 1,000,000 instructions per second.

The central processor unit (CPU) consists of six logic modules. Using only one basic set of standard printed-circuit boards, word lengths of 16, 24 or 32 bits are attained via component population of the logic modules. Under firmware control, these modules enable the CPU to dynamically change its word length from one operating mode to another.

AMPP core memory is configured from basic memory modules, which contain 16,384 18-bit words. Maximum processor addressing capability is 524,288 16-bit words or 262,144 32-bit words.

The AMPP enclosure is a 1-ATR package, with a volume of 0.87 cubic foot. This enclosure contains the CPU, power supply and up to four basic memory modules.

The unique combination of word size, microprogram control and superior throughput allows the AMPP to emulate existing Mil-E-5400 computers — faster than real-time.

FUNCTIONAL CHARACTERISTICS

- Full microprogram control
- A basic micro-instruction execution time of 150 nanoseconds
- Up to 3K of ROM 64-bit micro-memory
- A word size of 16, 24 or 32 bits
- 750-nanosecond core memory
- Direct addressing to 262K 32-bit words
- Throughput in excess of 1,000,000 instructions per second

- I/O — Word length — Parallel channel
  Serial Channel, 2 MHz (Manchester coded)
  Serial GSE channel
- Instruction Repertoire: Emulation of existing instruction sets with attendant software savings
  Custom designed to fit applications

OPTIONS PRESENTLY AVAILABLE

- Multi-bank memory for overlapping instruction and operand fetch
- Up to four independent memory access ports
- 1K high-speed semiconductor instruction/operand memory
- High-speed floating point hardware
- Program-loadable counters/real-time clock
- Memory parity/storage protect
- Specialized I/O for system applications
- High-speed, 63-place, single pass shift matrix

SPECIFICATIONS

Processor —

Type: General purpose, parallel microprogrammable digital processor
Organization: Register oriented or file oriented
Word Length: 16, 24 or 32 bits
Micromemory Type: Semiconductor, ROM or ROM/RAM combination
Micromemory Size: Configured in increments from 512 to 3K 64-bit microinstructions
Micromemory Cycle Time: 150 nanoseconds (average)
Arithmetic: Binary, with 1's or 2's complement, fixed or floating point
Registers: Up to 512 (word length) file registers

Main Memory —

Core Storage: 2½" D, 3 wire; configured in 16K x 18-bit increments (16 data, 1 parity and 1 protect); up to 262K x 36 bits
Cycle Time: 750 nanoseconds
Access Time: Maximum 450 nanoseconds with 4 memory ports
Addressing Mode: Determined by microprogram; flexible to suit application
Storage Protect: Optional by word
Parity: Optional

Input/Output —

I/O Channels: parallel, serial, DMA (optional). Others to suit customer application

General —

Interrupts: 16 internal, 8 external (or to suit application); programmable priority
Program Loadable Counters: 2-8 second program loadable/readable counters (0.5 microseconds resolution)
Number of Instructions: 2^{63} (determined by user)
Average Instruction Rate (Gibson Mix): Approximately 1 MIP
Built-in Test: Greater than 95% detection of failure

Physical Characteristics —

Construction: ATR Modular
Size (inches): 7.62 x 10.125 x 19.56
Volume: 0.87 cu. ft.
Weight: 48 lbs. minimum configuration
65 lbs. maximum configuration
Power: MIL-STD-704A, Cat. B, 115 VAC, 400 Hz, three phase, 450 watts min. Power consumption is a function of processor configuration and memory reference rate
Cooling: Parallel Forced Air Conduction

Environmental Design

MIL-E-5400 Class 2X
Temperature: —55°C to +71°C (operating)

Shock: 15g, 3 axis 11 millisec, half sine wave
Vibration: MIL-E-5400 Curve IV
Humidity: Up to 100% operating or non-operating
EMI: MIL-STD-461 Notice 3 for Class 1C equipment
Altitude: Up to 70,000 feet
Sand and Dust: MIL-E-5400, Class 2X
Salt Spray: MIL-E-5400, Class 2X
Acoustical Noise: MIL-E-5400, Class 2X
MTBF: Basic 16K/32-bit; airborne inhabited — greater than 1,000 hours
MTTR: Fifteen minutes

GROUND SUPPORT EQUIPMENT

Basic ground support equipment (19" relay rack mounting) —

- Display/control panel and associated logic
- Remex cassette tape with cassette drive unit
- Display monitor panel with CRT display

Options —

- Console desk-unit mounting
- One or two additional cassette drive units with same controller
- One additional display monitor
- Teletype hard copy interface
- Commercial peripheral channel interface

AEROSPACE DIVISION
3101 EAST 80TH STREET, MINNEAPOLIS, MINNESOTA
MAILING ADDRESS • BOX 609, MINNEAPOLIS, MINNESOTA 55440

June 29, 1973

Raytheon Company
Electromagnetic Systems Division
6380 Hollister Avenue
P.O. Box 1542
Goleta, CA 93017

Attention: Mr. Richard White

Ref: Request for Proposal NK:73:058
Signal Processor Controller

Gentlemen:

In response to the above referenced RFP, Control Data Corporation is pleased to submit the attached proposal for Signal Processor Controllers.

Control Data is proposing to use the CDC Airborne Microprogrammable Processor, (AMPP). This approach, which utilizes state of the art design and components, meets or exceeds the requirements for the Signal Processor Controllers as set forth in Raytheon Statement of Work MAS:73:042.

Of significant importance is the fact that both the Transmitter and Receiver Controllers are packaged in a single enclosure, thereby reducing size, weight, power consumption and cost. This configuration will provide one complete ship set.

Pricing information will be submitted by TWX Monday July 2, 1973.

If you have any questions concerning the information contained in this proposal, please contact Mr. R. T. Peller 612/853-5520.

Very truly yours,

CONTROL DATA CORPORATION
Aerospace Division

Michael L. Fisher
Program Manager

RTP:cc

Enc.

RAYTHEON

DIVISION Electromagnetic Systems

Department

Classification Unclassified

Contract No.

Distribution See below

To THOSE LISTED

File No. pt

From O. Lowenschuss

Memo No. 73:OL:120

Subject Digital Computer Pricing Guide II

Date 21 December 1973

In a telephone conversation with Mike Fisher, CDC, December 21, 1973, he provided the following data:

The prices below are for quantities of 200, in accordance with MIL-STD-883, level B. For quantities of 1,000, subtract 10%. For quantities of 50, add 20%.

CPU, 16 bits; four cards, including 1K ROM plus master interconnection board. $20,000.00

CPU, 32 bits, same as above (four cards, etc.) $22,000.00

ROM, 16 bits wide; basic price $ 1,100.00

For each 1K of ROM, add $600 to maximum of 8K.

RAM, basic price, $1100.00. For each 1K, add $1350, to maximum of 6K.

Core memory: 16K by 16 bits; basic price for memory controller module (handles four core memory banks), single bank single port: $3,000.

Core memory itself, 16K by 16 bits: $12,000.00.

Enclosure, front panel, no lights, connectors: $3,000.00.

Power supply for machine that includes core memory, $7,500.00.

CDC has checked this with the 32 bit AMPP version (CDC 5670, replacement for SKC-2070), and states that the prices are within a few dollars. However, for the small controllers, receiver controller and transmitter controller of B-1, prices calculated in this manner are about twice what they would be in accordance with the current quote.

O. Lowenschuss

cc: W. Barquist, P. Jacobs, R. Riel, J. Weiss

PRODUCT EXCELLENCE PROGRAM